Design Impact of BEOL LER

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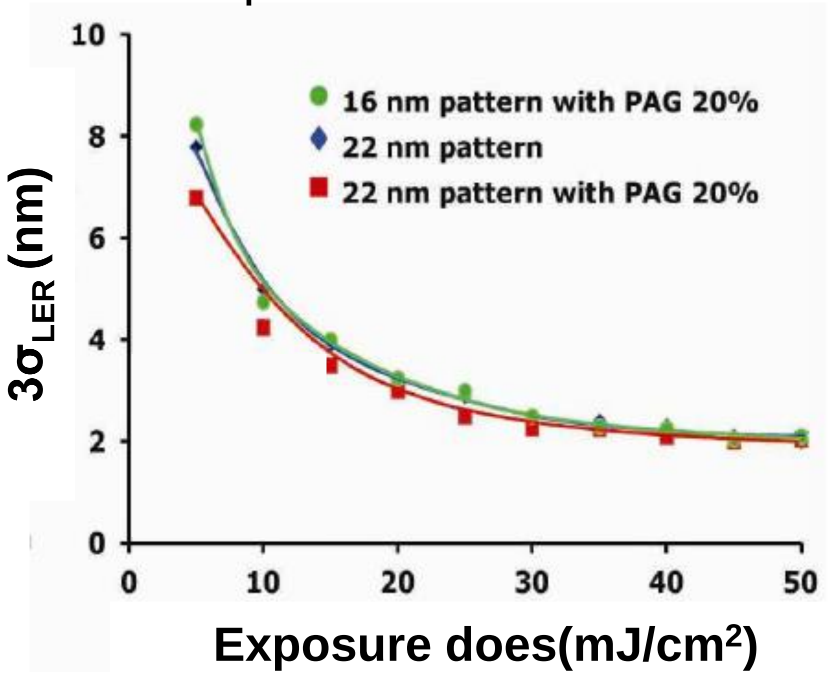
LER in EUV Lithography

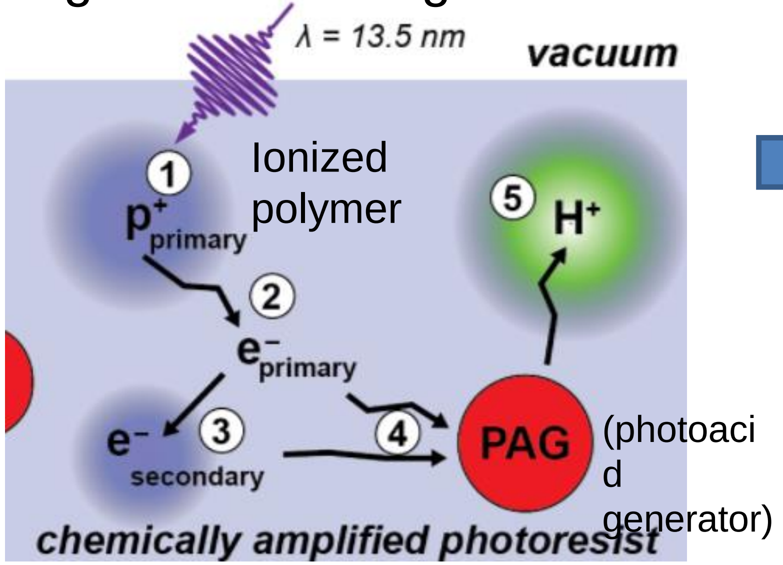
Photon shot noise

- Limited EUV light source power
- Less photon count



Photoelectrons and secondary electrons

- Ionization by high energy photons
- High diffusion length

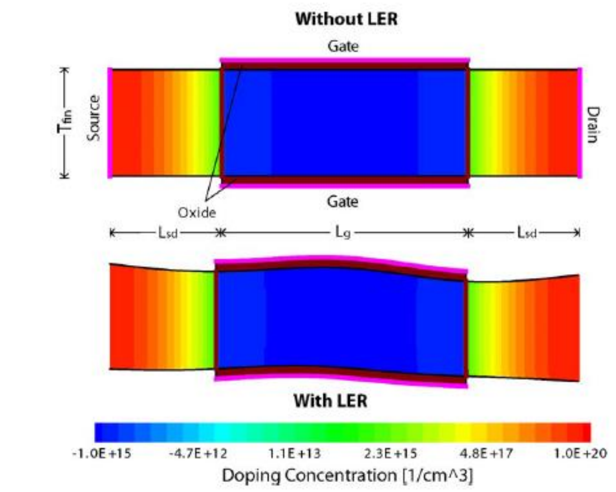


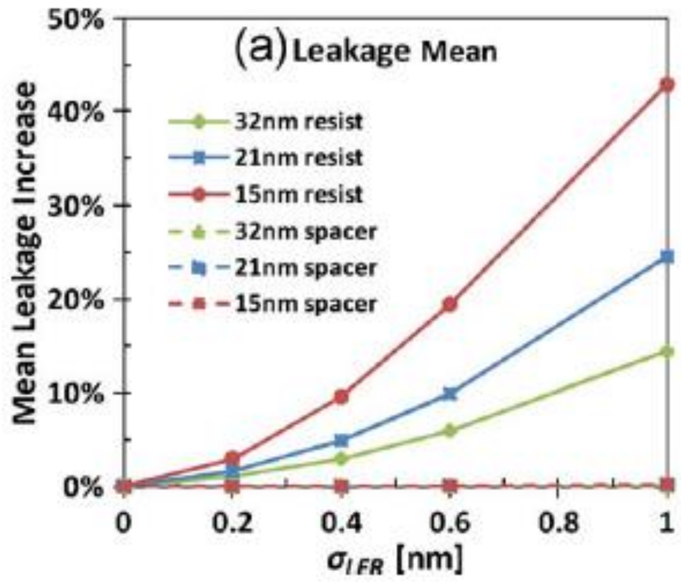
Higher LER in EUV

Ref: 1. Kim, Sang-Kon. "Modeling and Simulation of Line Edge Roughness for EUV Resists." JSTS: Journal of Semiconductor Technology and Science 14.1 (2014): 61-69.
2. Mojarad, Nassir, Jens Gobrecht, and Yasin Ekinci. "Beyond EUV lithography: a comparative study of efficient photoresists' performance." Scientific reports 5 (2015): 9235.
3. https://amolf.nl/research-groups/euv-photoemission/research-activities-2

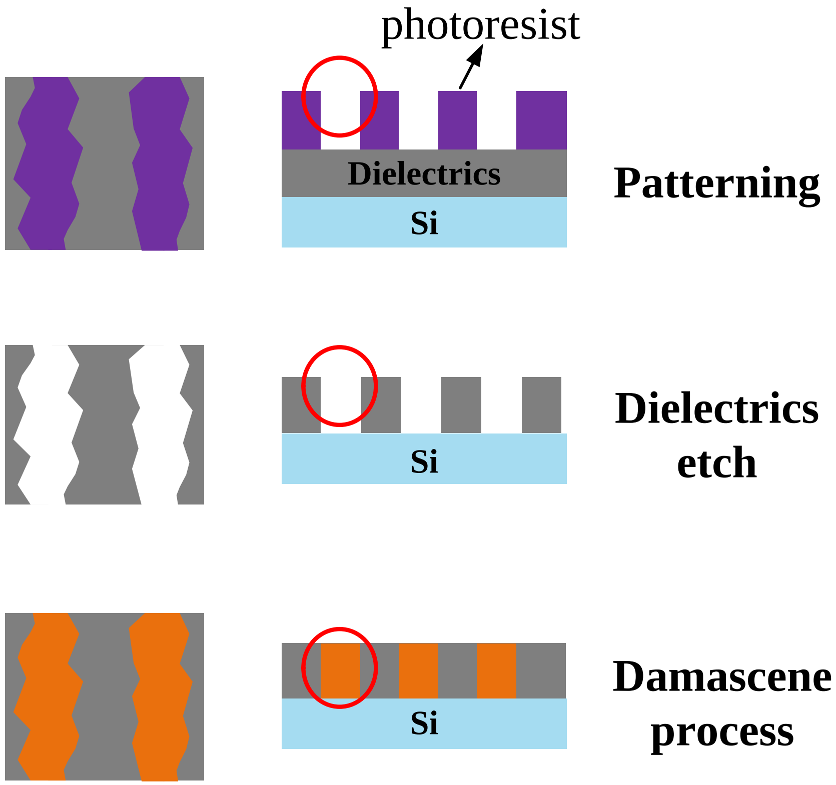
LER Impact in Front End

- Can use NRG models to estimate impact of gate LER.
- Fin LER in FinFETs → fin thickness variation
  - "spacer defined fins" → correlated LER → little LWR
  - "resist defined fins" → uncorrelated LER → high LWR
- Impact on delay is small (averaging effect)
- Impact on leakage power large for resist defined fins
  - Similar results for planar devices as well
- *Lot* of work on LER analysis for devices → focus on BEOL in this talk
  - G. Leung, L. Lai, P. Gupta, and C. O. Chui, "Device- and Circuit-Level Variability Caused by Line Edge Roughness for Sub-32nm Finfet Technologies," *IEEE Transactions on Electronic Devices*, vol. 59, pp. 2057 -2063, aug. 2012.

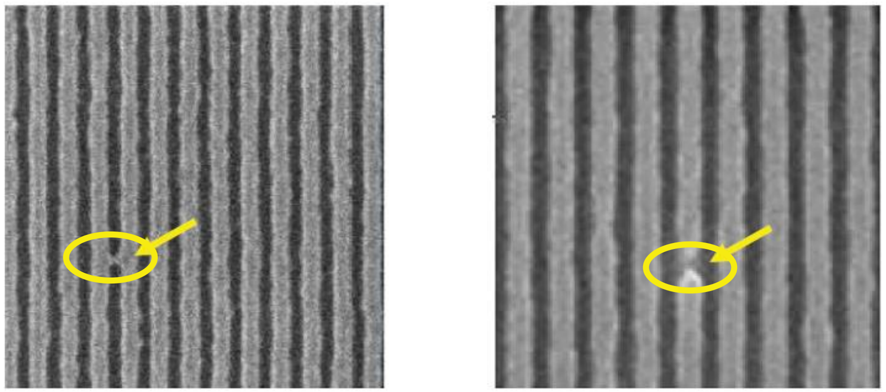




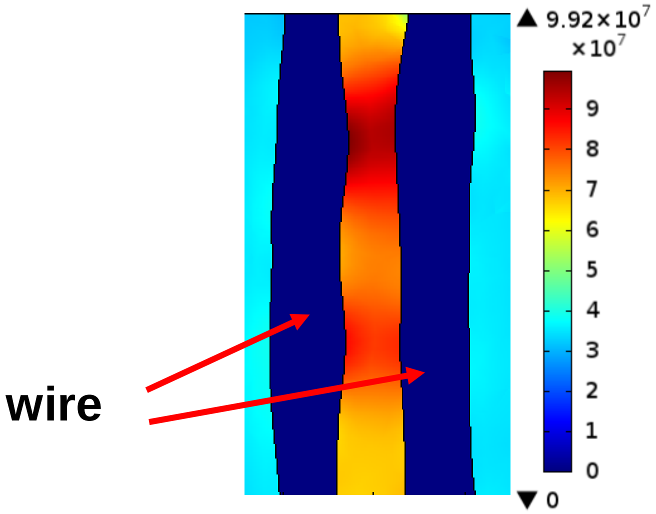
LER Induced Interconnect Failures



LER transferred from photoresist to Cu wires



The space patterned by EUV



Electrical field intensity distribution

Wire shorts/opens

Enhanced TDDB failure

- Lower yield
- Higher EUV light source power required

Modeling LER Impact

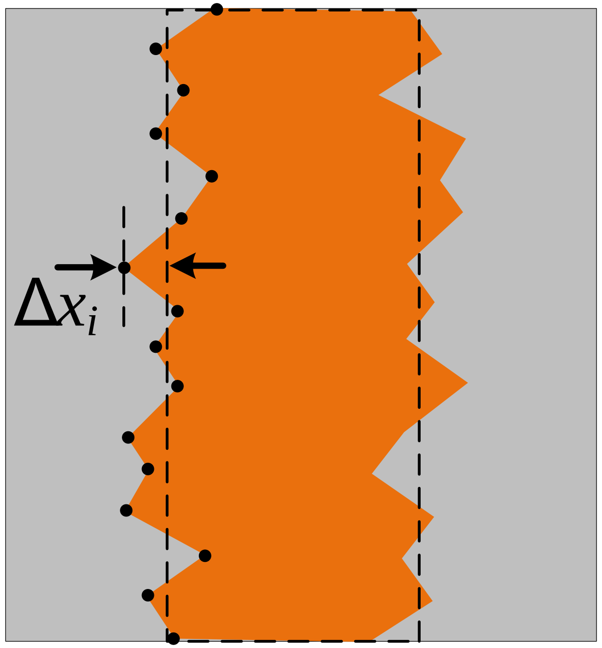
Y. Luo and P. Gupta, “Relaxing ler requirement in euv lithography,” in *SPIE Advanced Lithography*, March 2018.

LER model

- Parameters to characterize LER
  — standard deviation: σ_{LER}
  — correlation length: λ
- Power spectral density (PSD) of LER
  — Gaussian or exponential autocorrelation function
- Analytical approach to model LER
  — Sample LER magnitude ($\Delta x_1, \Delta x_2, \ldots \Delta x_N$) with interval 1nm
  — Δx_i : Gaussian random variables N(0,σLER)
  — Spatial correlation

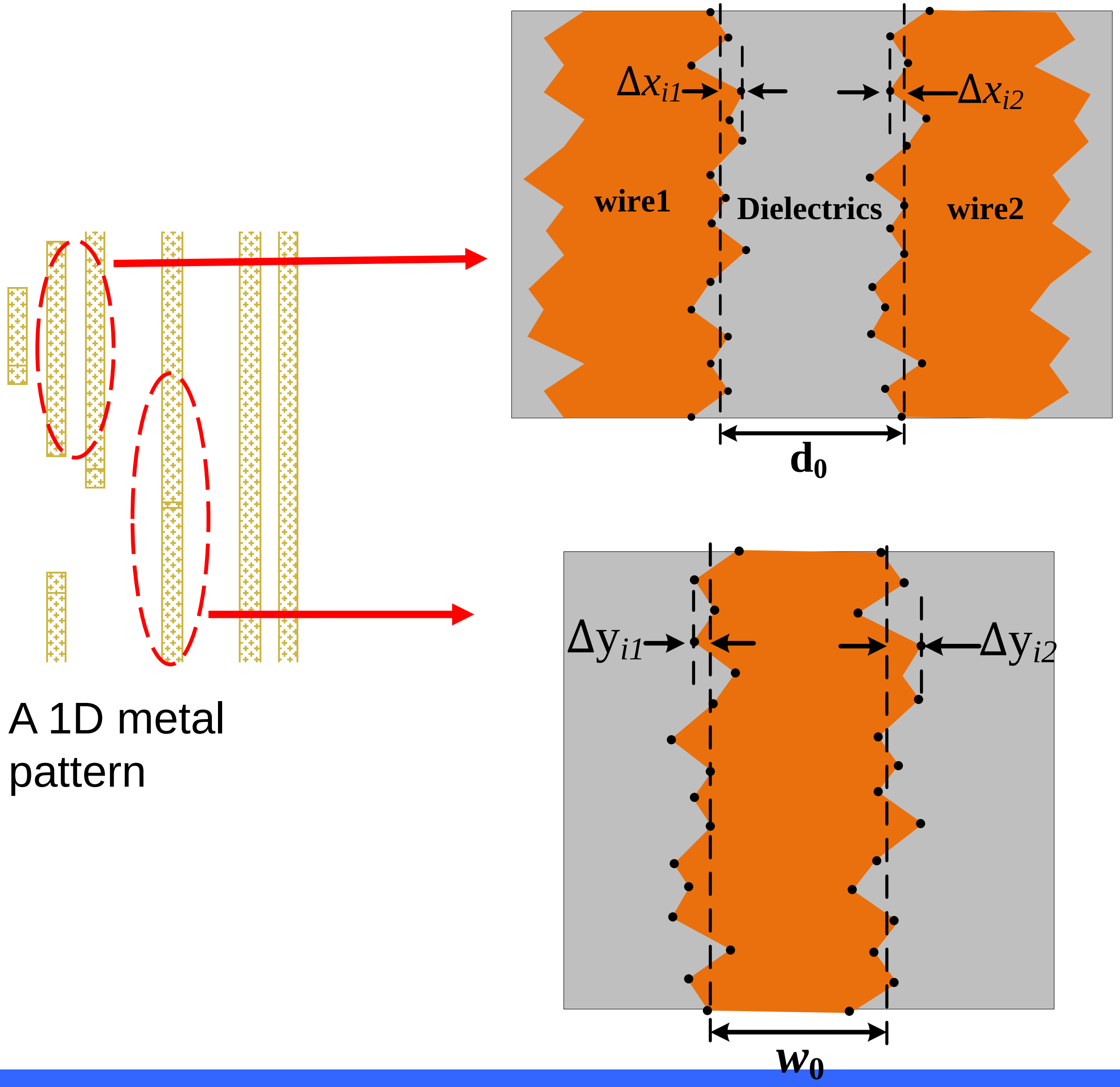
$$\mathrm{cov}(\Delta x_i, \Delta x_j) = \sigma_{LER}^2 \exp\left(-\frac{\left[(i-j)dx\right]^2}{\lambda^2}\right)$$

N-dimension Gaussian distribution



LER along a metal wire

Failure Probability



A 1D metal pattern

Short Probability

$$P\left(short, L_n\right) = 1 - \underbrace{P(X_1 < d_0, X_2 < d_0, \ldots, X_N < d_0)}_{\text{No metal micro-bridging in the dielectrics}}$$

$X_i = \Delta x_{i1} + \Delta x_{i2}$: size of LER protrusion in the dielectrics

Open probability

$$P(open, L_n) = 1 - \underbrace{P(Y_1 < w_0, Y_2 < w_0, \ldots, Y_N < w_0)}_{\text{No wire cutting}}$$

Where $Y_i = \Delta y_{i1} + \Delta y_{i2}$ is the size of LER defects in the wire

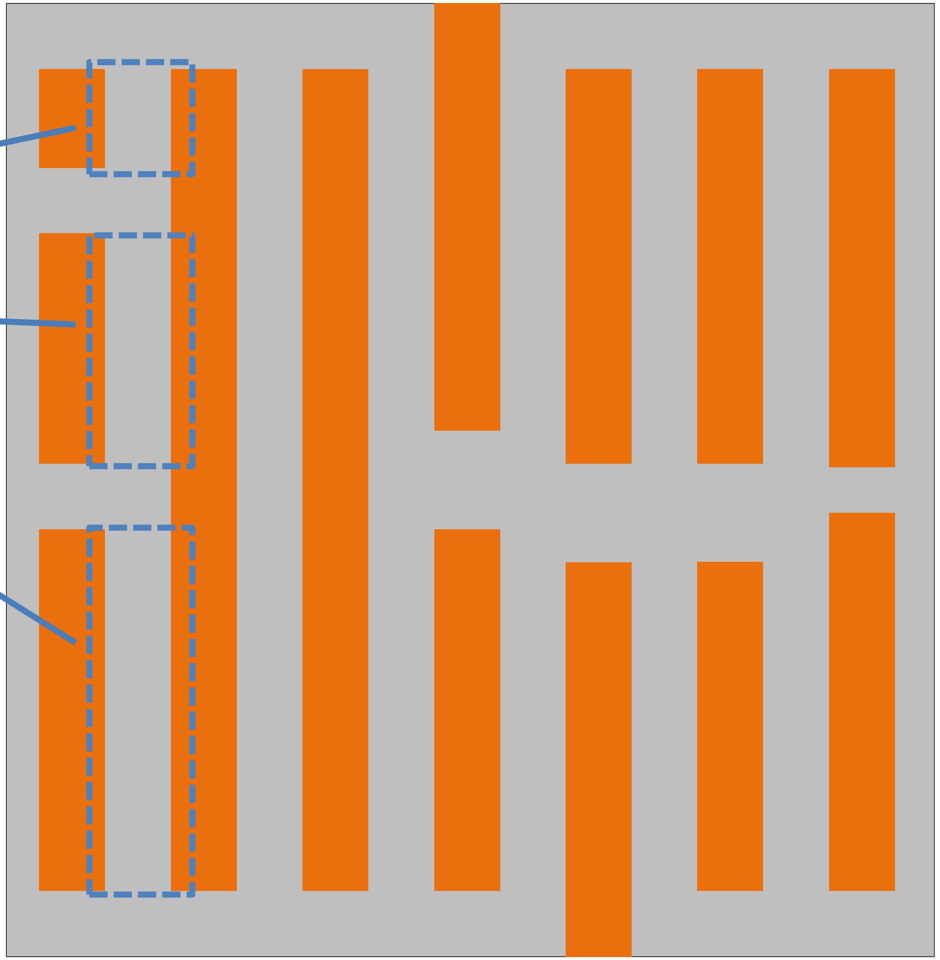
Estimating Chip Level Failures

- Chip level short probability

$$P(short) = 1 - \underbrace{\prod_{m=1}^{N} (1 - P(short, L_m))}_{\text{No short occurs among all the overlap regions}}$$

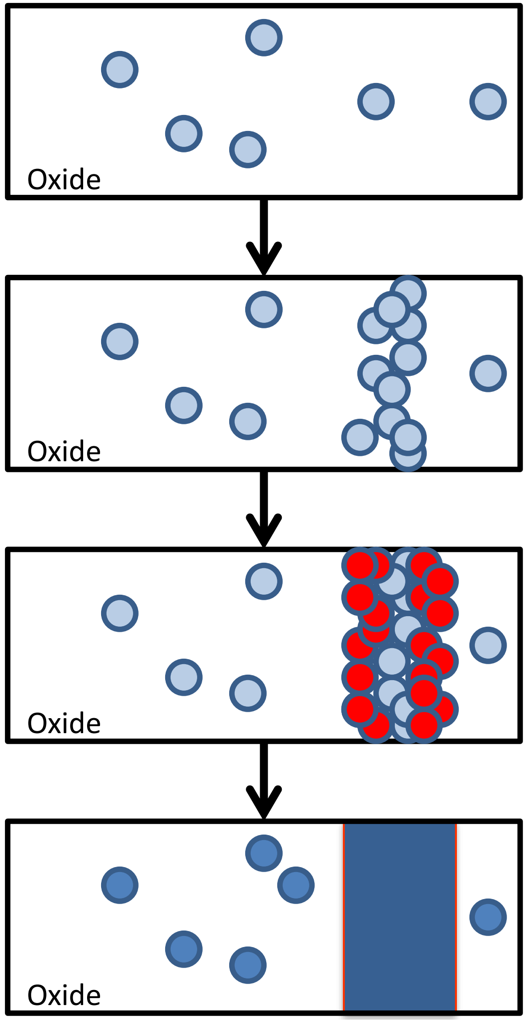
- Chip level open probability

$$P(open) = 1 - \underbrace{\prod_{m=1}^{N_{wire}} (1 - P(open, L_m))}_{\text{No open occurs among all the metal wires}}$$



Metal layer with 1D pattern

Time Dependent Dielectric Breakdown (TDDB)



- TDDB refers to the destruction of a dielectric (1) at gate oxide or (2) between metal lines
  - Oxide defects accumulates over time
  - Overlapping defects form conductive path → Soft breakdown happens
  - Conduction leads to heat → thermal damage → more defects → more conduction
  - Oxide in the breakdown spots melts
  - Conductive filament is formed
  - Hard breakdown happens
- TDDB worsened by higher electric field between metal lines due to reduced spacing from LER

LER-aware TDDB model

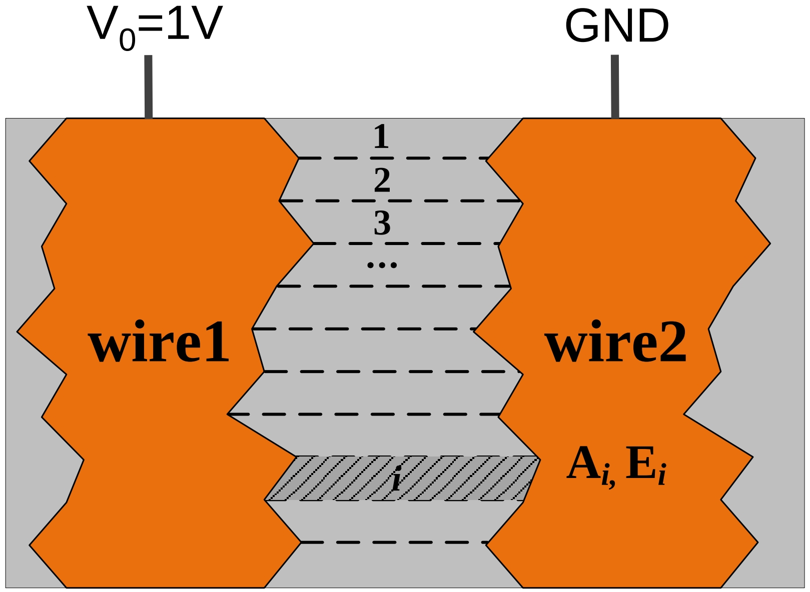
- Probability of TDDB before time *t*

$$F(t) = 1 - \exp\left[-\left(\frac{t}{\eta(E, A)} \right)^{\beta} \right]$$

Weibull slope

Characteristic lifetime

- The dielectrics are segmented



Dielectrics segmentation

- The chip-level TDDB estimation

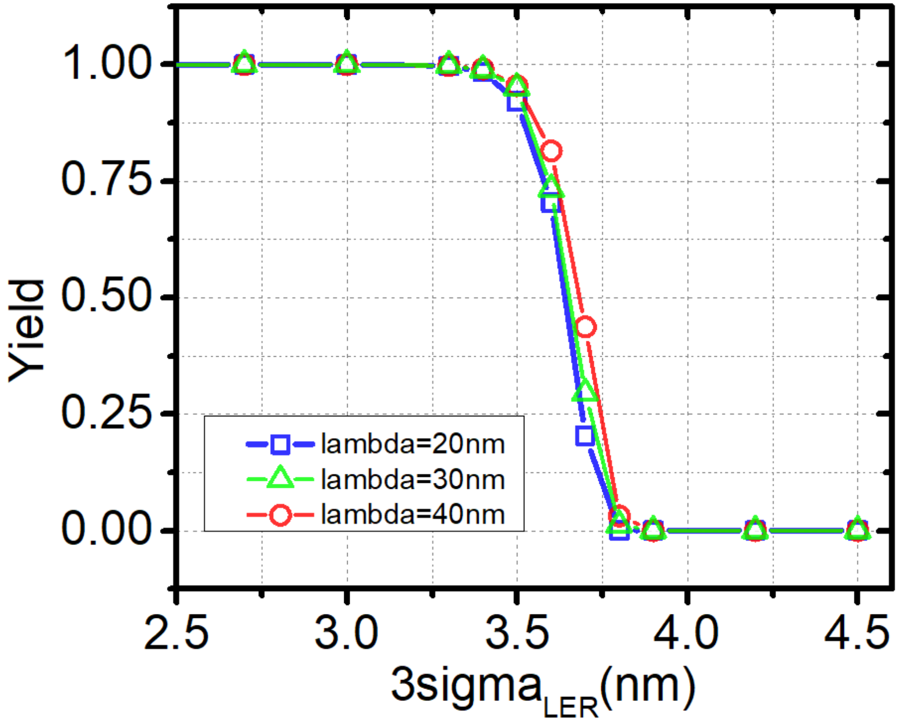
$$F(t) = 1 - \underbrace{\prod_{i=1}^{N} \left(1 - F_i(t)\right)}_{\text{No dielectrics fails}} = 1 - \prod_{i=1}^{N} \exp\left[-\left(t / \eta_i(E_i, A_i)\right)^{\beta} \right]$$

E-field in the i^{th} segment

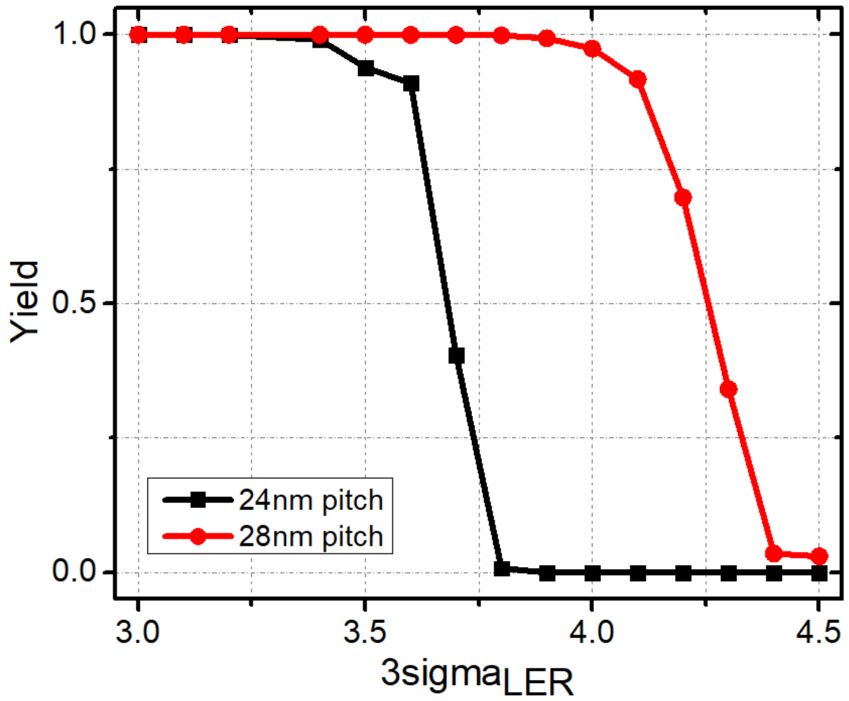
Dielectric area of the i^{th} segment

Example LER Case Studies

Single Patterning EUV



- Layout: Grating with 24nm pitch
- 1cm×1cm chip
- Yield reduced to 0.99 at $3\sigma_{LER}$=3.4nm

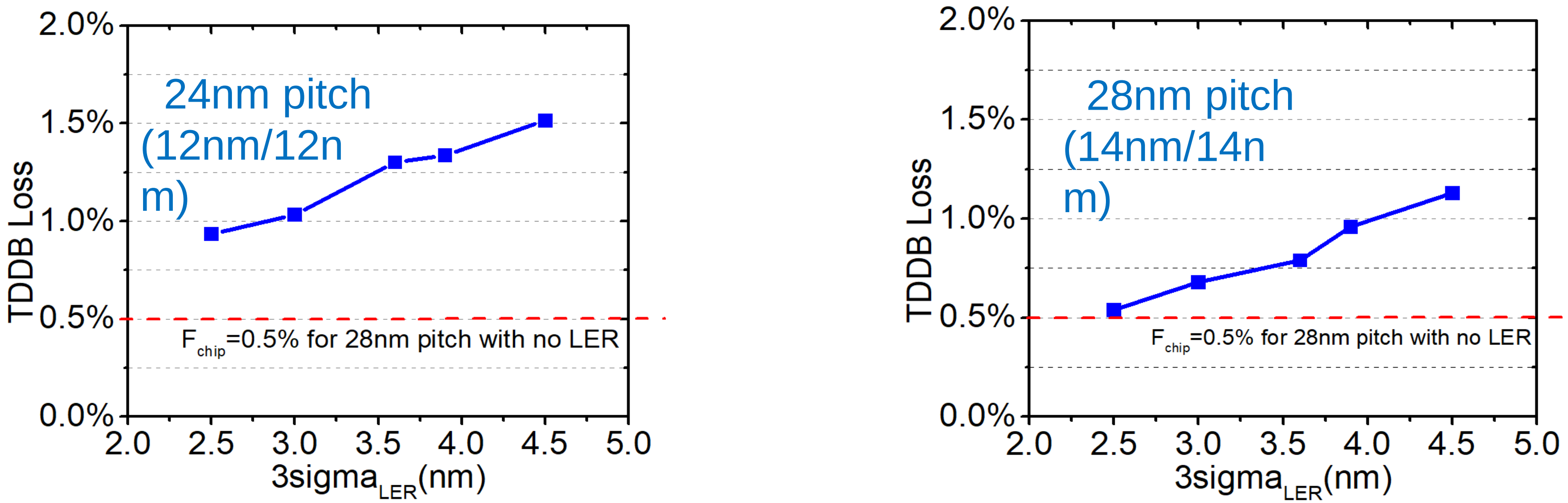


- Layout: M1 of CORTEXM0
  - Scale down the layout to 5nm-node
  - The metal pitch is scaled down to 24nm or 28nm
  - The total track utilization > 75%

Single patterning EUV acceptable LER < 3.4nm

5-Year TDDB Loss

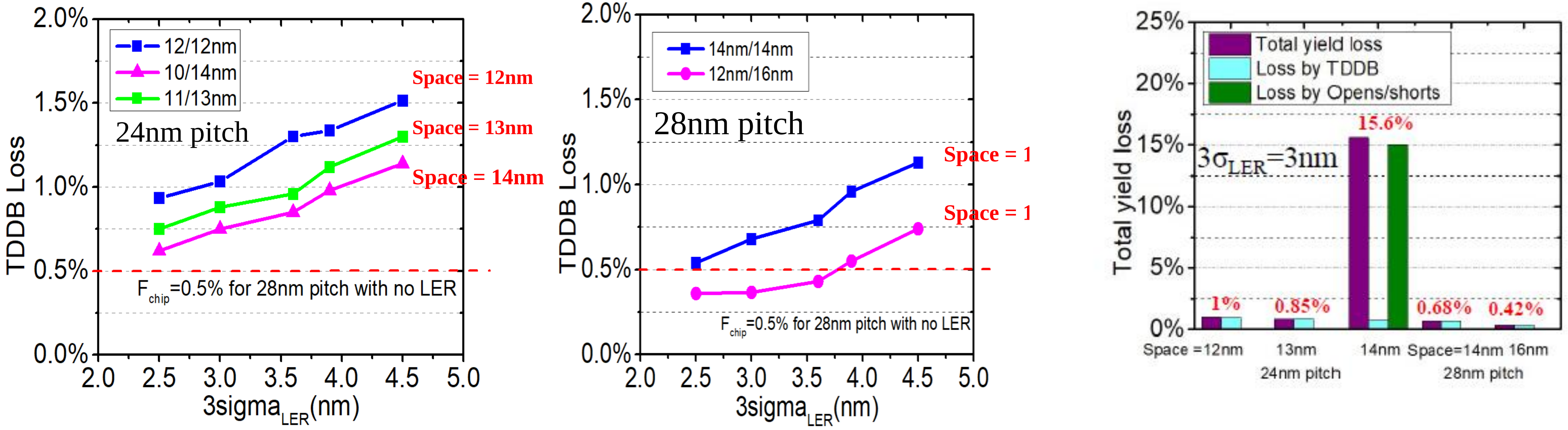
- TDDB loss: fraction of chips getting reliability field return
  - *Much* more costly than yield loss



5-year TDDB loss

2X worsening of reliability at 3.4nm LER → acceptable LER with TDDB < 3nm

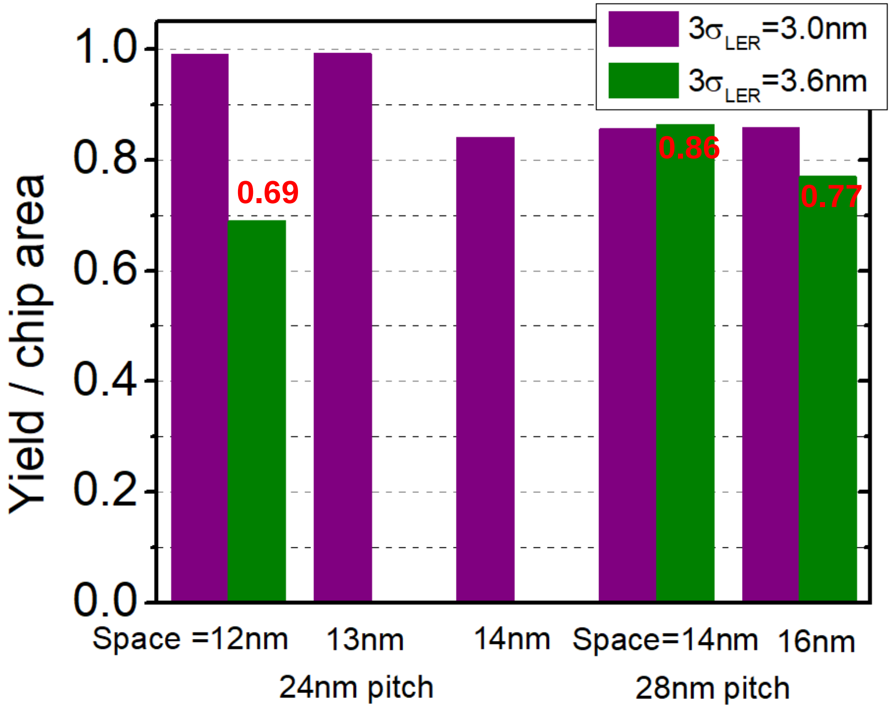
TDDB Mitigation with Design Rule Changes



- Increase space → reduced electric field → reduced TDDB *but* worse opens: yield-reliability tradeoff
  - Cannot have too much asymmetry in width/spacing at constant pitch
    - Pitch dictates layout density and shrink
- ***3nm LER with 13nm spacing at 24nm a sweet spot***

The Overall Yield Picture

- Two solutions to LER
  - Reduce LER!
  - Increase wire pitch
    - Tradeoff between design area and yield

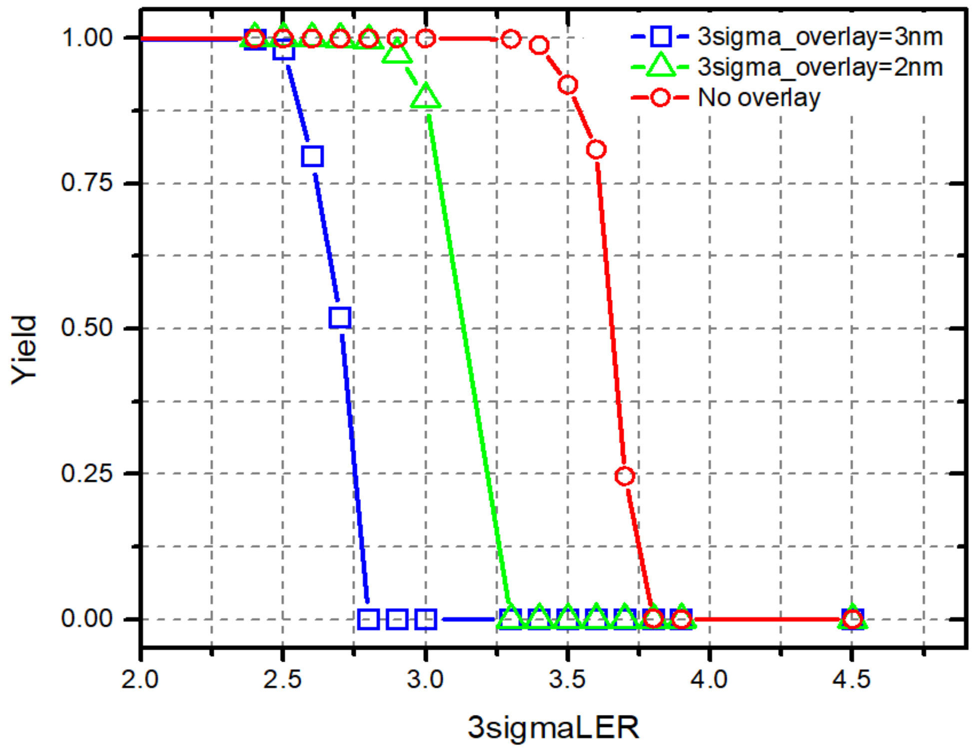


Yield/chip area

About 15% chip area penalty to maintain high yield

A Note on EUV Multiple Patterning

- Overlay eats into the LER budget
- ***2nm overlay error → reduction of acceptable LER by 1nm***



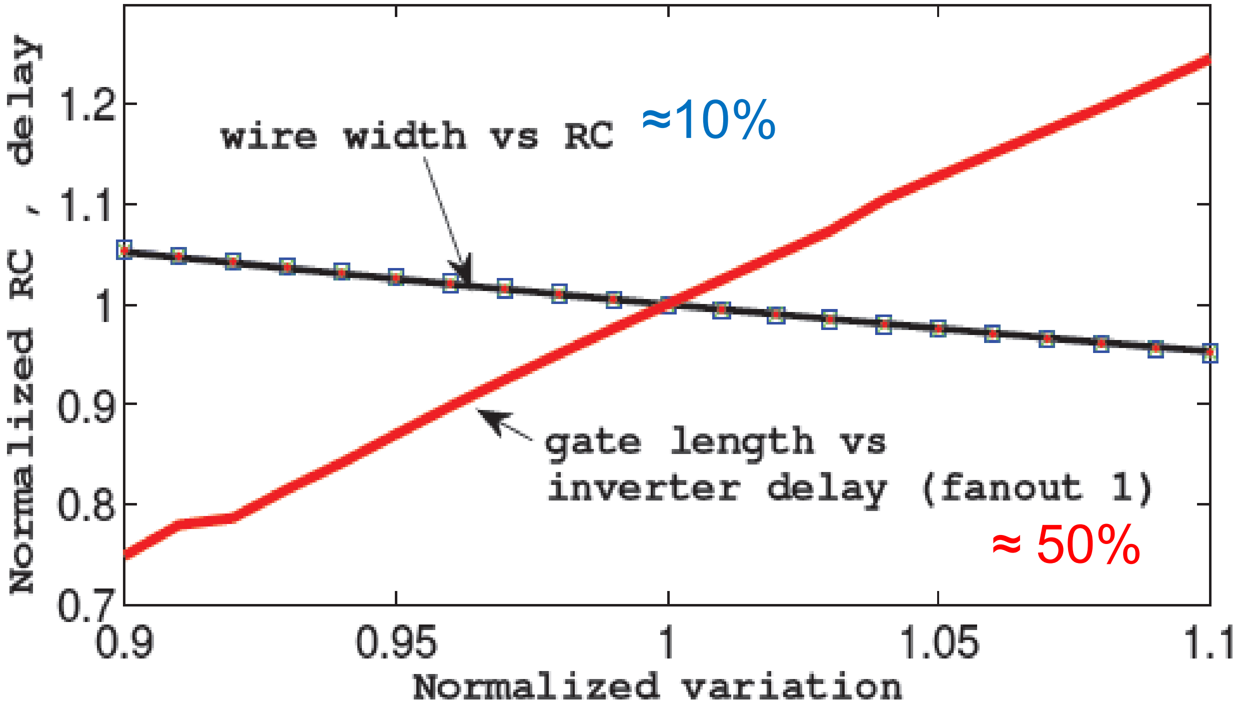
Performance Impact of BEOL LER

Is Interconnect Modeling Important ?

- Probably not..
  - Litho impacts wire width↑↓ (w)
    - w↑ → R_{wire}↓, C_g↑, C_c↑
  - Wire_Delay ~ 0.5*R_{wire}*(C_g + C_c + C_L) ~ $K_1 + \frac{K_2}{w(P-w)} + \frac{K_3}{w}$
  - Gate_Delay ~ R_{gate}*(C_g + C_c + C_L) ~ $\frac{K_4}{P-w} + K_5 w + K_6$
  - Wires are *long* → averaging effects
  - Semi-global and global wiring (M3+) is wide and regular → patterning less of an issue
  - M1/M2 impact on power/performance is small
  - Caveat: contacts (and via) R variation may be non-negligible

Why Wires Are Not As Important

- Width variation averages over long wires.
- Resistance and capacitance change in opposite directions as line width changes.



FreePDK 45nm process

Simulation at Chip-Level

- Delay and switching power <3%.
- Impact of wire variation is exaggerated as averaging effect is ignored.

Interconnect layers (variation)	Δ delay (%)	Δ Switching power (%)
M2 (+10%)	0.89	1.46
M2 (-10%)	-0.75	-0.69
M3 (+10%)	1.90	2.83
M3 (-10%)	-1.62	-1.85
M4 (+10%)	0.77	1.64
M4 (-10%)	-0.65	-0.84
M5 (+10%)	0.08	0.50
M5 (-10%)	-0.07	0.13
M6 (+10%)	0.22	0.65
M6 (-10%)	-0.19	0.00

Total gates=43K Total area=0.2mm^2

FreePDK 45nm process

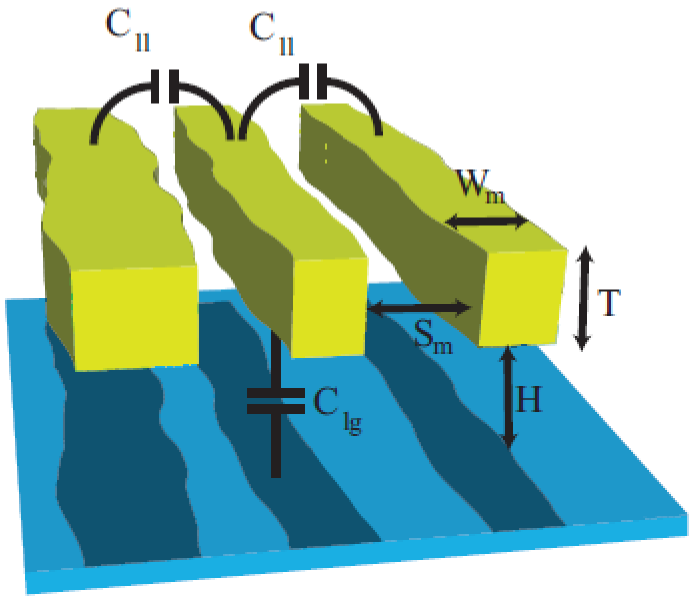
Chip performance estimation

- Evaluate the impact of design rule change on chip performance
- Elmore's delay model

$$t_{0.5} = k\left[0.7R_{drv}\left(C_g + 4.4C_c + C_{drv}\right) + R_w\left(C_g + 1.5C_c + 0.7C_{drv}\right)\right] \qquad \text{(No buffer)}$$

$$t_{0.5} = k\left[0.7\frac{R_{drv}}{h}\left(\frac{C_g}{k} + 4.4\frac{C_c}{k} + hC_{drv}\right) + \frac{R_w}{k}\left(0.4\frac{C_g}{k} + 1.5\frac{C_c}{k} + 0.7hC_{drv}\right)\right] \qquad \text{(Buffered)}$$

- Wire geometry variation on resistance and Capacitance
- Dimension dependent Cu resistivity model

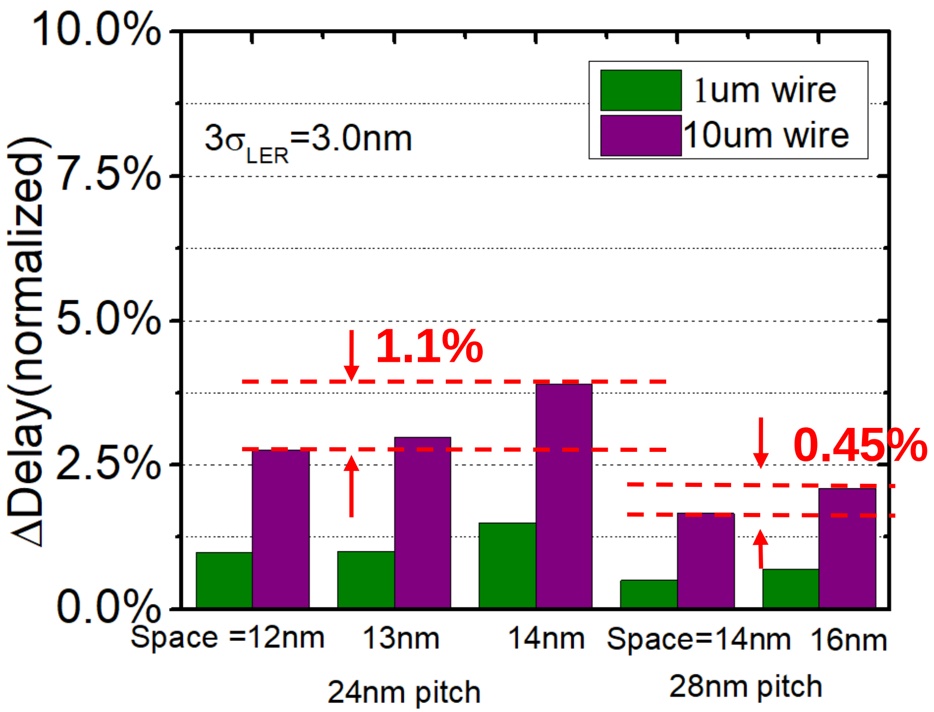


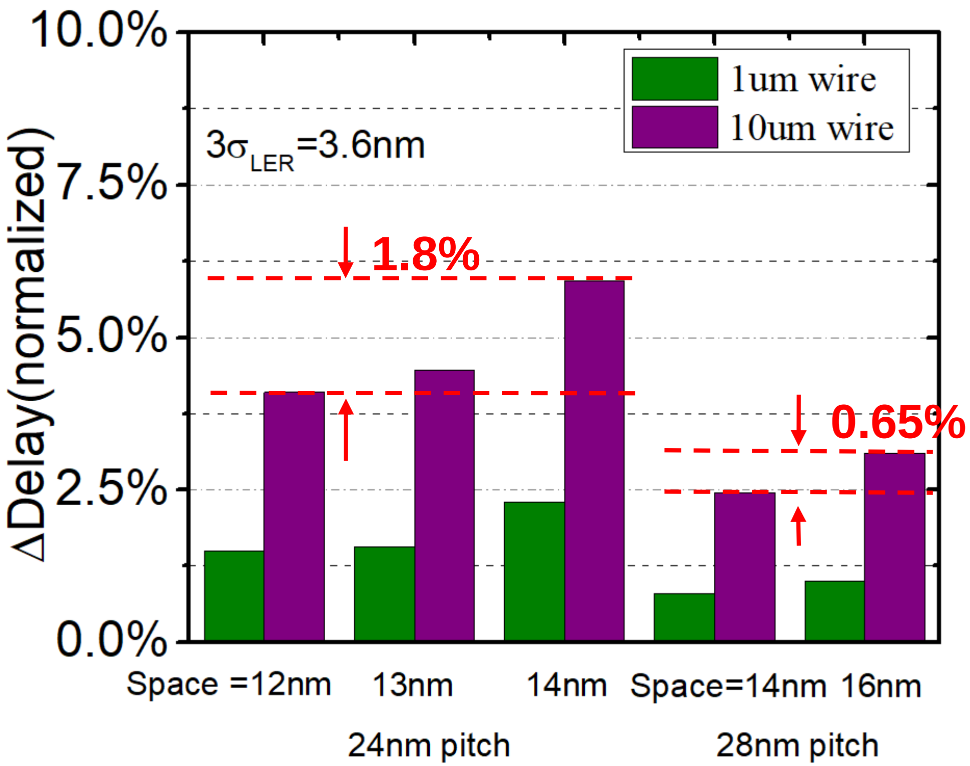
Wire geometry with LER

Ref: 1. Twaddle, F. J., et al. "RC variability of short-range interconnects." *Computational Electronics, 2009. IWCE'09. 13th International Workshop on*. IEEE, 2009.

Chip performance estimation

- Delay mainly attributed to the LER induced wire geometry variation



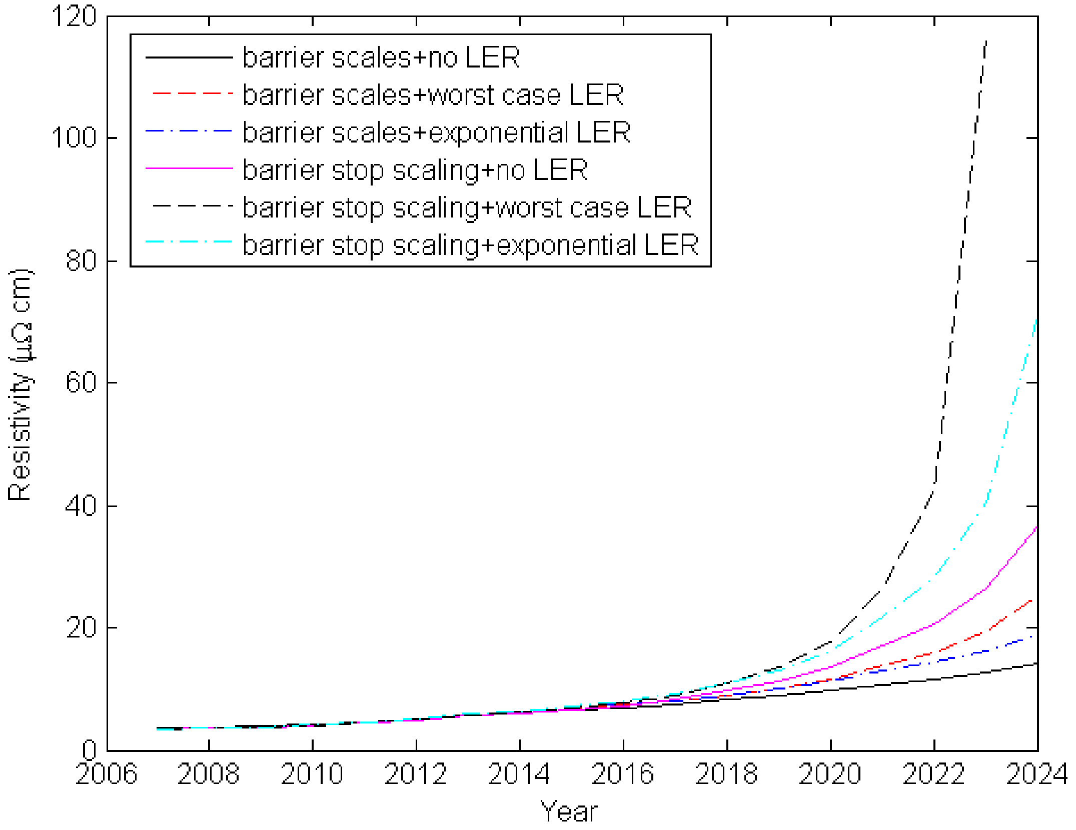


Delay increment at $3\sigma_{LER}$=3nm and 3.6nm

Design rule change has small impact on delay

Caveat: Cu Barrier Scaling

- LER for local wires can be critical as amount of copper is small due to barrier that is difficult to scale
- Large resistivity impact
  - Assume ITRS dimensions
  - Assume barrier may stop scaling at 1.9nm
- Capacitance impact is small
- RC impact 10%-40%



Conclusions and Future work

Conclusions

- LER requirements can be harsh for EUV (<3nm for single patterning and <2nm for multiple patterning)
- Some relaxation possible by smarter optimization of design rules
  - Use larger spacing than width
- Performance impact of BEOL LER is not a first order concern

Future work

- Need to look into LER impact on contacts/vias, trim, block…

Thank you